TRANSISTOR CHARACTERISTICS

BJT:

Junction transistor,

Transistor current components,

Transistor equation,

Transistor configurations,

Transistor as an amplifier,

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Common Emitter and Common Collector configurations,

Ebers-Moll model of a transistor,

Punch through/ reach through,

Photo transistor,

Typical transistor junction voltage values

FET:

FET types, construction, operation, characteristics, parameters,

MOSFET-types, construction, operation, characteristics,

Comparison between JFET and MOSFET.

Transistor:

A bipolar junction transistor (BJT) is a three terminal device in which operation depends on the interaction of both majority and minority carriers and hence the name bipolar. It is used in amplifier and oscillator circuits, and as a switch in digital circuits. It has wide applications in computers, satellites and other modern communication systems.

Transistor = Trans + istor

Trans means signal transfer property of the device and istor means belong to the family of resistors. A transistor consists of 3 terminals. They are,

1. Emitter (E)
2. Base (B) and
3. Collector (C).

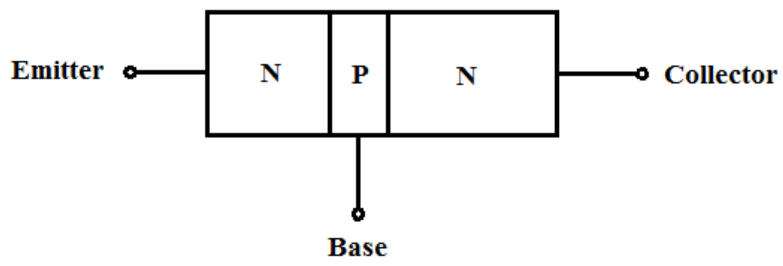
Emitter which emits the charge carriers, collector collects the charge carriers through base. In order to emit the charge carriers emitter is heavily doped, collector is moderately doped and base is lightly doped. The width of collector is more compared to base and emitter. Base width is very small compared to emitter. Collector width is made wider than emitter in order to dissipate the heat produced whenever it collects the charge carriers.

BJT's are classified into two types. They are

1. NPN transistor
2. PNP transistor

NPN Transistor:

The semi conductor representation and symbolic representation of an npn transistor is shown in the following figure.



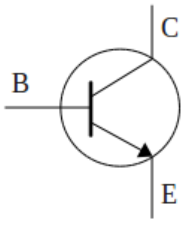


Figure: Semi conductor representation of npn transistor Figure: Symbolic representation of npn transistor

From the diagram an npn transistor is constructed by sandwiching a p type semi conductor between two n-type semi conductors. Here we have two n-type semi conductors and one p type semi conductor, hence the majority charge carriers in npn transistor is electrons and minority charge carriers are holes. Current is produced by both majority and

minority charge carriers. The arrow mark in the symbol represents the conventional current direction.

Biasing:

On order to emit the charge carriers, emitter is always forward biased and to collect the charge carriers collector is connected in reverse bias. The biasing of npn transistor is shown below.

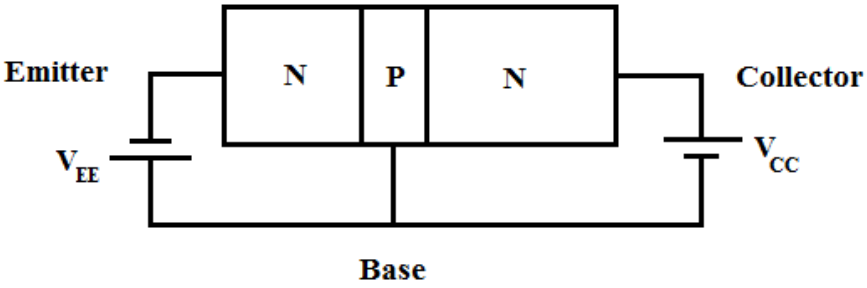


Figure: Biasing of npn transistor

Working:

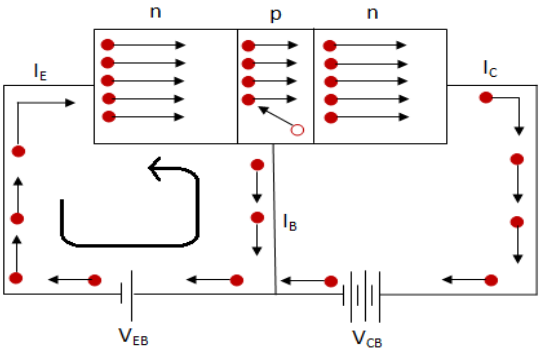


Figure: Working of npn transistor

If the transistor is connected as per the above biasing. Charge carriers (electrons) from emitter will move towards collector. N-type emitter is connected to the negative terminal of the battery, the charge carriers will repel from that moves towards base and attracted towards n-type collector is connected to positive terminal of the battery. If we take emitter base junction, it is forward biased. The conventional current direction is shown in the above figure. Means in the transistor symbol arrow represents the conventional current direction.

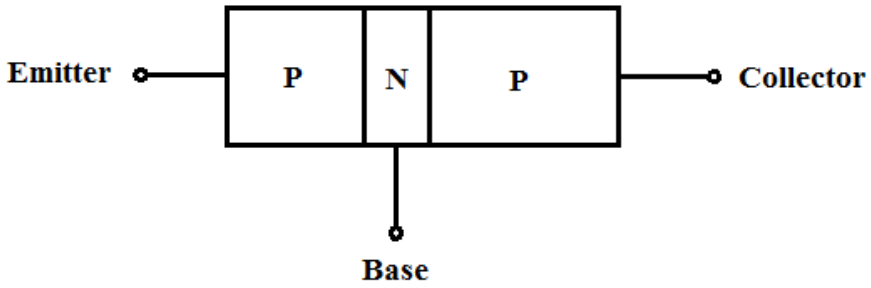
The total emitter current is the sum of base and collector currents.

$$I_E = I_B + I_C$$

If we assume emitter current is 100%, then base current is 10% and collector current is 90%.

PNP Transistor:

The semi conductor representation and symbolic representation of an npn transistor is shown in the following figure.



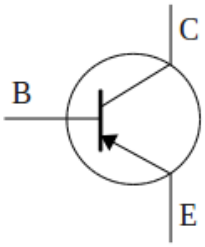


Figure: Semi conductor representation of pnp transistor Figure: Symbolic representation of pnp transistor

From the diagram an pnp transistor is constructed by sandwiching a n type semi conductor between two p-type semi conductors. Here we have two p-type semi conductors and one n type semi conductor, hence the majority charge carriers in pnp transistor is holes and minority charge carriers are electrons. Current is produced by both majority and minority charge carriers. The arrow mark in the symbol represents the conventional current direction.

Biasing:

On order to emit the charge carriers, emitter is always forward biased and to collect the charge carriers collector is connected in reverse bias. The biasing of pnp transistor is shown below.

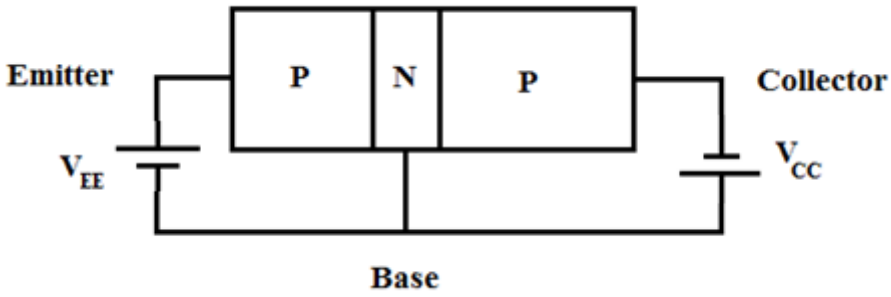


Figure: Biasing of npn transistor

Working:

If the transistor is connected as per the above biasing. Charge carriers (holes) from emitter will move towards collector. p-type emitter is connected to the positive terminal of the battery, the charge carriers will repel from that moves towards base and attracted towards p-type collector is connected to negative terminal of the battery. If we take emitter base

junction, it is forward biased. The conventional current direction is shown in the above figure. Means in the transistor symbol arrow represents the conventional current direction.

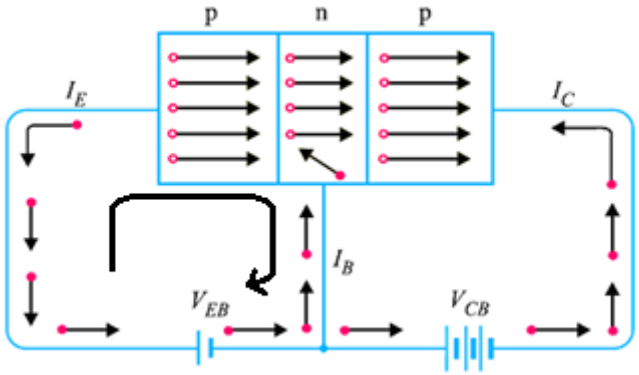


Figure: Working of pnp transistor

The total emitter current is the sum of base and collector currents.

$$I_E = I_B + I_C$$

If we assume emitter current is 100%, then base current is 10% and collector current is 90%.

Transistor Current components:

The current components in a transistor when emitter is forward biased and collector is reverse biased. The emitter current is the sum of hole current I_{pE} (holes from emitter to base) and electron current I_{nE} (electrons from base to emitter). The ratio of hole to electron current I_{pE}/I_{nE} is proportional to the conductivity of p type to n type material.

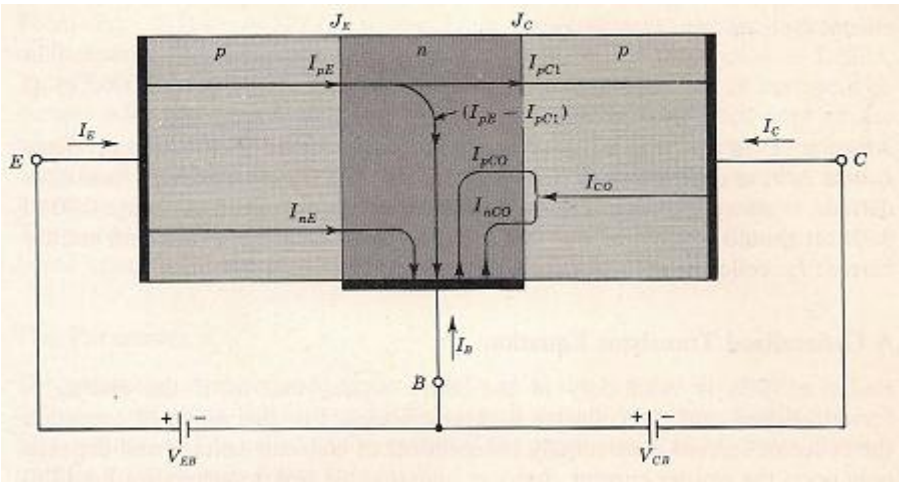


Figure: Current components in a transistor

I_{pE} and I_{nE} are the diffusion currents. Then the minority carrier diffusion currents crossing the junction is represented as $I_{pE}(0)$ and $I_{nE}(0)$.

The total current crossing the junction is $I=I_{pE}+I_{nE}$

When the holes moves towards the collector junction, they will recombine with the electrons in the base. The current because of holes after recombination is I_{pC1}. The recombination hole current is $I_{pE} - I_{pC1}$.

Let us consider the emitter is open circuited, collector junction remains reverse biased. Then the reverse saturation current I_{CO} flows and it consists of two components, I_{nCO} and I_{pCO}.

- $I_{CO} = I_{nCO} + I_{pCO}$

Since, I_E=0, no holes reaches to collector, then I_{pCO} results from the small concentration of holes generated thermally in the base.

$I_C = I_{CO} – I_{pC1} = I_{CO} - \alpha I_E$

α is defined as the fractional of the total emitter current.

Large Signal Current gain (α):

It is defined as the ratio of the negative of the collector-current increment from cutoff to the emitter current change from cutoff.

$$\alpha = -\frac{I_C - I_{CO}}{I_E - 0}$$

α is called as the large signal current gain. It lie in the range 0.9 to 0.95.

Transistor Equation:

The generalized transistor, replace I_{CO} with the current in the diode.

$$I_C = -\alpha I_E + I_{CO}\left(1 - e^{V_C/V_T}\right)$$

In the above equation, I_O is replaced with - I_{CO} and V is replaced with V_C.

If V_C is very large, then e^{V_C/V_T} is very small and neglected.

$$I_C = -\alpha I_E + I_{CO}$$

We know that, I_E= - (I_C+I_B)

$$I_C = -\alpha\left(-(I_C + I_B)\right) + I_{CO}$$

$$I_C = \alpha I_C + \alpha I_B + I_{CO}$$

$$I_C(1 - \alpha) = \alpha I_B + I_{CO}$$

$$I_C = \frac{\alpha}{(1 - \alpha)} I_B + I_{CO}$$

$$I_C = \beta I_B + \frac{1}{(1-\alpha)} I_{CO}$$

$$I_C = \beta I_B + (1+\beta) I_{CO}$$

$$Since, \beta = \frac{\alpha}{1-\alpha}$$

Transistor Configurations:

In order to construct a circuit, we need two input and two output terminals. Whereas a transistor has only 3 terminals. Hence, one terminal is made as common to input and output. Accordingly, we have three terminals, so we have three types of configurations. They are

1. Common Base configuration
2. Common Emitter configuration
3. Common Collector configuration

If we consider a simple two port network, we have input current, input voltage, output current and output voltage. Out of the four parameters, two are taken as independent and two are taken as dependent parameters for the convenience.

Dependent Parameters: Input Voltage, Output Current

Independent Parameters: Input Current, Output Voltage

Input Voltage = f(Input Current, Output Voltage)----------(1)

Output Current=f(Input Current, Output Voltage)----------(2)

Equation 1 is helpful for obtaining the input characteristics and 2 for output characteristics.

Common Base (CB) configuration:

In common base configuration, base is common to input and output. The circuit diagram for CB configuration is shown below.

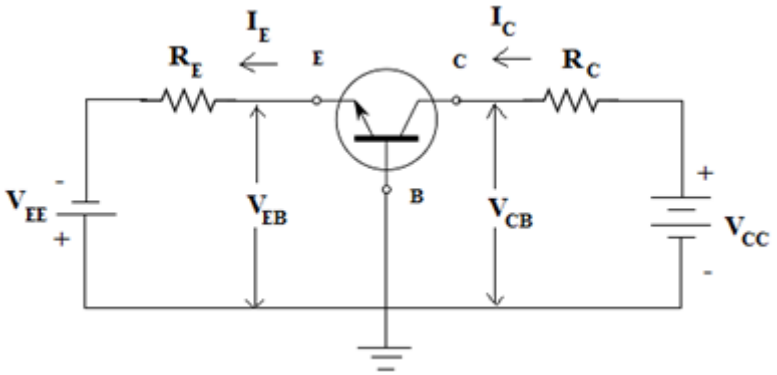


Figure: Circuit Diagram of CB configuration

Here the input is applied between the base and emitter terminals and the corresponding output signal is taken between the base and collector terminals with the base terminal grounded. Here the input parameters are V_{EB} and I_E and the output parameters are V_{CB} and I_C. The input current flowing into the emitter terminal must be higher than the base current and collector current to operate the transistor, therefore the output collector current is less than the input emitter current.

The input parameters are V_{EB}, I_E and the output parameters are V_{CB} and I_C.

$$V_{EB} = f(I_E, V_{CB}) \text{ ---------(1)}$$

$$I_C = f(I_E, V_{CB}) \text{ ---------(2)}$$

Input Characteristics

Equation1 is used for plotting input characteristics. Input characteristics are obtained between input current and input voltage with constant output voltage. First keep the output voltage V_{CB} constant and vary the input voltage V_{EB} for different points then at each point record the input current I_E value. Repeat the same process at different output voltage levels. Now with these values we need to plot the graph between I_E and V_{EB} parameters. The below figure show the input characteristics of common base configuration.

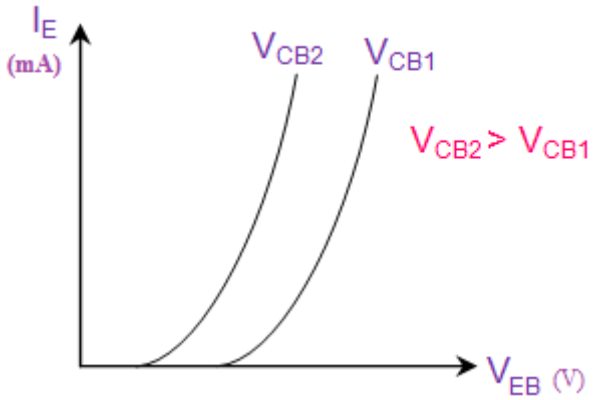


Figure: Input Characteristics of CB configuration

If reverse bias voltage of C-B junction is keep on increasing, a situation arises where E-B and C-B space charge regions touch each other, and the width of the quasi-neutral base region becomes zero, Known as base punch through.

As there is an increase in collector voltage, depletion width increases, this in turn decreases effective base width. This is called as early effect.

Output Characteristics

Equation2 is used for plotting output characteristics. The output characteristics of common base configuration are obtained between output current and output voltage with constant input current. First keep the emitter current constant and vary the V_{CB} value for

different points, now record the I_C values at each point. Repeat the same process at different I_E values. Finally we need to draw the plot between V_{CB} and I_C at constant I_E. The below figure show the output characteristics of common base configuration.

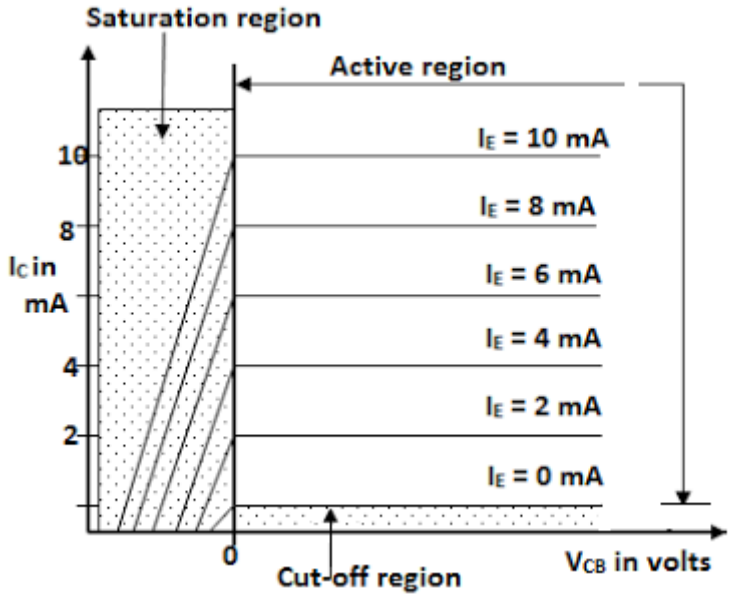


Figure: Output characteristics of CB configuration

Input Bias	***Output Bias***	***Region of operation***	***Application***
Reverse	Reverse	Cut off	OFF Switch
Forward	Reverse	Active	Amplifier
Forward	Forward	Saturation	ON Switch
Reverse	Forward	Inverse Active	Attenuator

Transistor parameters:

1. Input Resistance: $r_i = \frac{\Delta V_{EB}}{\Delta I_E} / V_{CB}\ Constant$

$$h_{ib} = \frac{\Delta V_{EB}}{\Delta I_E} / V_{CB}\ Constant$$

   Input resistance in Common Base is in the order of few ohms.

2. Output Resistance: $r_o = \frac{\Delta V_{CB}}{\Delta I_C} / I_E\ Constant$

$$h_{ob} = \frac{\Delta I_C}{\Delta V_{CB}} / I_E\ Constant$$

Output resistance in Common Base is in the order of hundred of kilo ohms.

3. Current Gain: $A_I = \frac{\Delta I_C}{\Delta I_E} / V_{CB}\ Constant$

$$\alpha = h_{fb} = \frac{\Delta I_C}{\Delta I_E} / V_{CB}\ Constant$$

Current gain is always less than unity.

4. Voltage Gain: $A_V = \frac{\Delta V_{CB}}{\Delta V_{EB}} / I_E\ Constant$

$$h_{rb} = \frac{\Delta V_{EB}}{\Delta V_{CB}} / I_E\ Constant$$

Voltage gain in common base configuration is high.

Common Emitter (CE) Configuration:

In common emitter configuration, emitter is common to input and output. The circuit diagram for CE configuration is shown below.

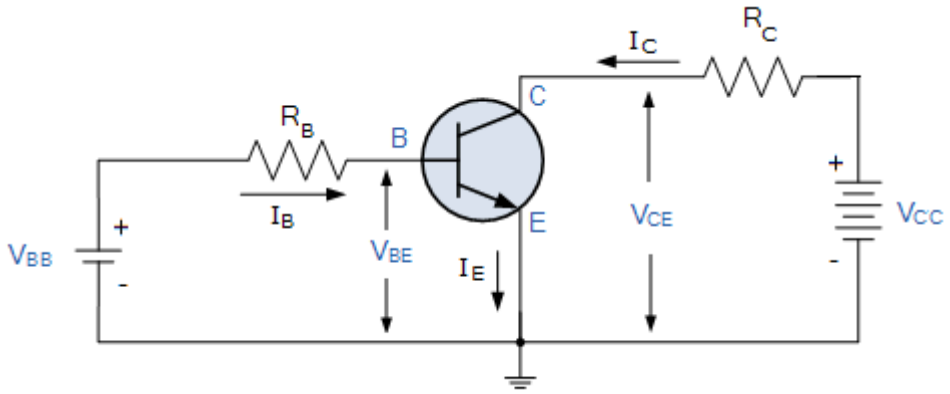


Figure: Circuit diagram for CE configuration

The input to the CE is applied to the base-emitter circuit and the output is taken from the collector-emitter circuit, making the emitter the element "common" to both input and output. The CE is set apart from the other configurations, because it is the only configuration that provides a phase reversal between input and output signals. This configuration is mostly used one among all the three configurations. It has medium input and output impedance values.

The input voltage and input current are V_{BE} and I_B. Output voltage and output current are V_{CE} and I_C. Then the equations used for plotting input and output characteristics are

$$V_{BE} = f(I_B, V_{CE}) \text{ ----------(1)}$$

$$I_C = f(I_B, V_{CE}) \text{ ----------(2)}$$

Input Characteristics:

Using equation1, the input characteristics of common emitter configuration are obtained between input current I_B and input voltage V_{BE} with constant output voltage V_{CE}. Keep the output voltage V_{CE} constant and vary the input voltage V_{BE} for different points, now record the values of input current at each point. Now using these values we need to draw a graph between the values of I_B and V_{BE} at constant V_{CE}.

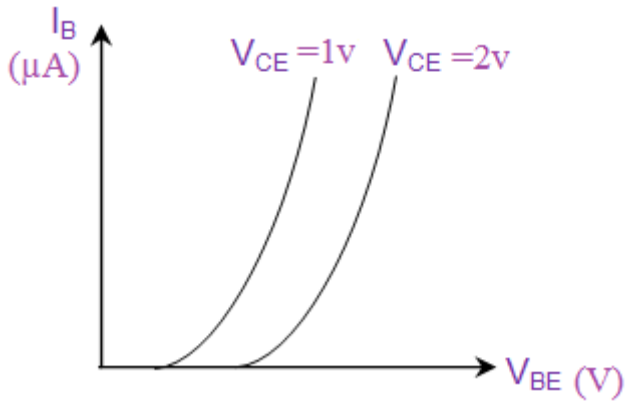


Figure: Input characteristics of CE configuration

Output Characteristics

Using equation2, the output characteristics of common emitter configuration are obtained between the output current I_C and output voltage V_{CE} with constant input current I_B. Keep the base current I_B constant and vary the value of output voltage V_{CE} for different points, now note down the value of collector I_C for each point. Plot the graph between the parameters I_C and V_{CE} in order to get the output characteristics of common emitter configuration.

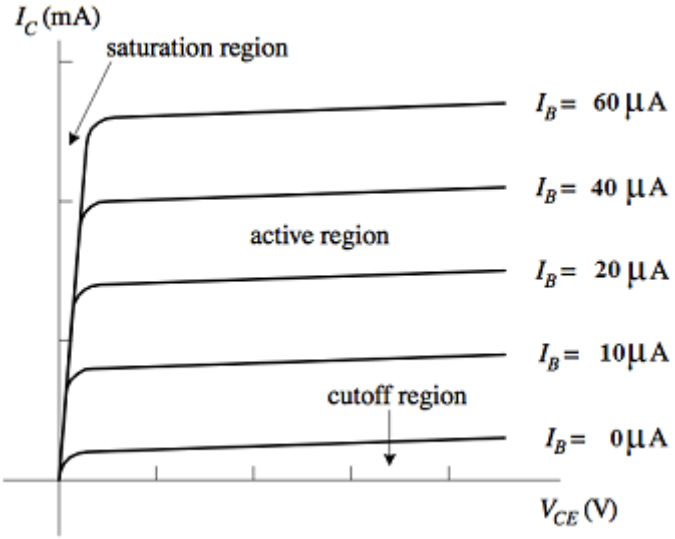


Figure: Output characteristics of CE configuration

Transistor parameters:

1. Input Resistance: $r_i = \frac{\Delta V_{BE}}{\Delta I_B} / V_{CE}\ Constant$

$$h_{ie} = \frac{\Delta V_{BE}}{\Delta I_B} / V_{CE}\ Constant$$

Input resistance in Common Emitter is moderate.

2. Output Resistance: $r_o = \frac{\Delta V_{CE}}{\Delta I_C} / I_B\ Constant$

$$h_{oe} = \frac{\Delta I_C}{\Delta V_{CE}} / I_B\ Constant$$

Output resistance in Common Emitter is moderate.

3. Current Gain: $A_I = \frac{\Delta I_C}{\Delta I_B} / V_{CE}\ Constant$

$$\beta = h_{fe} = \frac{\Delta I_C}{\Delta I_B} / V_{CE}\ Constant$$

Current gain in Common Emitter configuration is high.

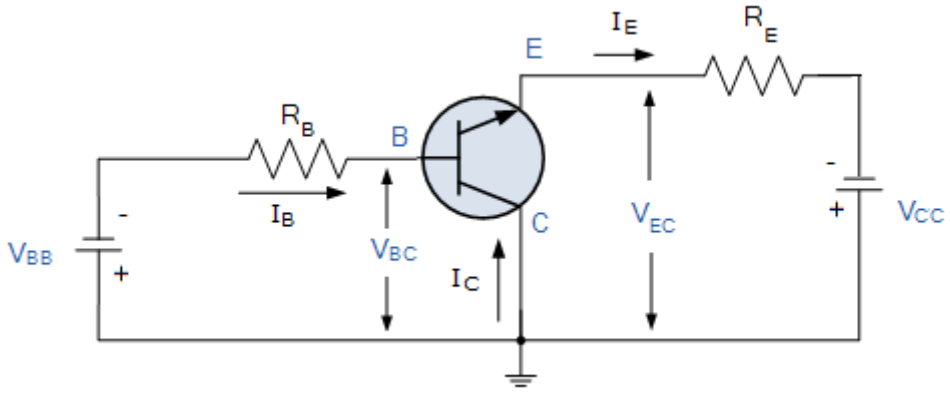
4. Voltage Gain: $A_V = \frac{\Delta V_{CE}}{\Delta V_{BE}} / I_B\ Constant$

$$h_{re} = \frac{\Delta V_{BE}}{\Delta V_{CE}} / I_B\ Constant$$

Voltage gain in common Emitter configuration is high.

Common Collector (CC) Configuration:

In common collector configuration, collector is common to input and output. The circuit diagram for CC configuration is shown below.



This configuration is also known as emitter follower configuration because the emitter voltage follows the base voltage. This configuration is mostly used as a buffer. These configurations are widely used in impedance matching applications because of their high input impedance.

The input voltage and input current are V_{BC} and I_B. Output voltage and output current are V_{EC} and I_E. Then the equations used for plotting input and output characteristics are

$$V_{BC} = f(I_B, V_{EC}) \text{ ----------(1)}$$

$$I_E = f(I_B, V_{EC}) \text{ ----------(2)}$$

Input Characteristics:

The input characteristics of a common collector configuration are quite different from the common base and common emitter configurations because the input voltage V_{BC} is largely determined by V_{EC} level. The input characteristics of a common-collector configuration are obtained between inputs current I_B and the input voltage V_{CB} at constant output voltage V_{EC}. Keep the output voltage V_{EC} constant at different levels and vary the input voltage V_{BC} for different points and record the I_B values for each point. Now using these values we need to draw a graph between the parameters of V_{BC} and I_B at constant V_{EC}.

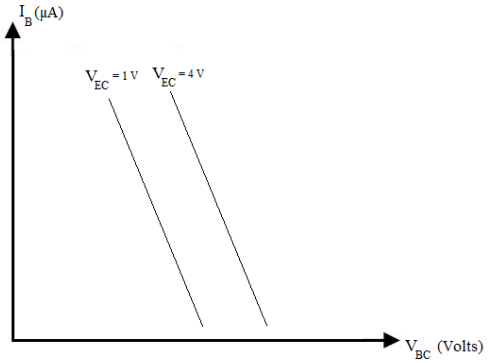


Figure: Input characteristics of CC Configuration

Output Characteristics:

The operation of the common collector circuit is same as that of common emitter circuit. The output characteristics of a common collector circuit are obtained between the output voltage V_{EC} and output current I_E at constant input current I_B. In the operation of common collector circuit if the base current is zero then the emitter current also becomes zero. As a result no current flows through the transistor. If the base current increases then the transistor operates in active region and finally reaches to saturation region. To plot the graph first we keep the I_B at constant value and we will vary the V_{EC} value for various points, now we need to record the value of I_E for each point. Repeat the same process for different I_B values. Now using these values we need to plot the graph between the parameters of I_E and V_{CE} at constant values of I_B. The below figure show the output characteristics of common collector.

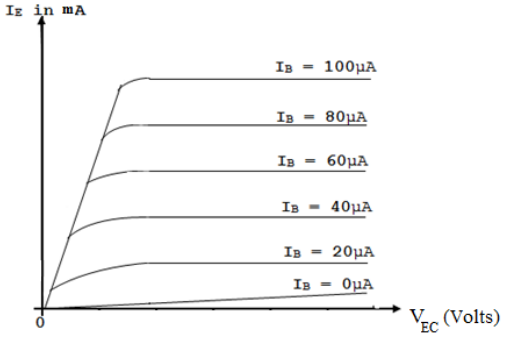


Figure: Output characteristics of CC Configuration

Transistor parameters:

1. Input Resistance: $r_i = \frac{\Delta V_{BC}}{\Delta I_B}/V_{EC}\ Constant$

   $$h_{ic} = \frac{\Delta V_{BC}}{\Delta I_B}/V_{EC}\ Constant$$

   Input resistance in Common collector is High.
2. Output Resistance: $r_o = \frac{\Delta V_{EC}}{\Delta I_E}/I_B\ Constant$

   $$h_{oc} = \frac{\Delta I_E}{\Delta V_{EC}}/I_B\ Constant$$

   Output resistance in Common collector is low.
3. Current Gain: $A_I = \frac{\Delta I_E}{\Delta I_B}/V_{EC}\ Constant$

   $$\gamma = h_{fc} = \frac{\Delta I_E}{\Delta I_B}/V_{EC}\ Constant$$

   Current gain in Common collector configuration is high.
4. Voltage Gain: $A_V = \frac{\Delta V_{EC}}{\Delta V_{BC}}/I_B\ Constant$

   $$h_{rc} = \frac{\Delta V_{BC}}{\Delta V_{EC}}/I_B\ Constant$$

   Voltage gain in common collector configuration is less than unity.

Amplification Factors:

In common Base configuration, $\alpha = \frac{\Delta I_C}{\Delta I_E}$

In common Emitter configuration, $\beta = \frac{\Delta I_C}{\Delta I_B}$

In common Collector configuration, $\gamma = \frac{\Delta I_E}{\Delta I_B}$

Relationship between α, β, and γ:

(i) Between α, β: We know that $\Delta I_E = \Delta I_B + \Delta I_C$

$$\alpha = \frac{\Delta I_C}{\Delta I_E} = \frac{\Delta I_C}{\Delta I_B + \Delta I_C} = \frac{\Delta I_C/\Delta I_B}{(\Delta I_B + \Delta I_C)/\Delta I_B} = \frac{(\Delta I_C/\Delta I_B)}{1 + (\Delta I_C/\Delta I_B)} = \frac{\beta}{1+\beta}$$

$$\beta = \frac{\alpha}{1-\alpha}$$

(ii) Between β and γ:

$$\beta = \frac{\Delta I_C}{\Delta I_B} = \frac{\Delta I_E - \Delta I_B}{\Delta I_B} = \frac{\Delta I_E}{\Delta I_B} - 1 = \gamma - 1$$

$$\gamma = 1 + \beta$$

(iii) Between γ and α:

$$\alpha = \frac{\Delta I_C}{\Delta I_E} = \frac{\Delta I_E - \Delta I_B}{\Delta I_E} = 1 - \frac{\Delta I_B}{\Delta I_E} = 1 - \frac{1}{\gamma} = \frac{\gamma - 1}{\gamma}$$

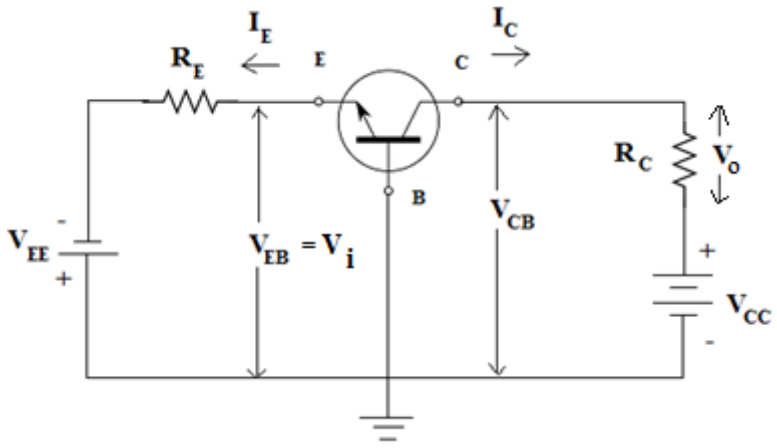
$$\gamma = \frac{1}{1 - \alpha}$$

Comparison of transistor configurations:

Parameter	***CB***	***CE***	***CC***
Input Resistance	Low	Moderate	High
Output Resistance	High	Moderate	Low
Current Gain	Less than unity	High	High
Voltage Gain	High	High	Less than unity
Amplification factor	$\alpha = \frac{\Delta I_C}{\Delta I_E}$	$\beta = \frac{\Delta I_C}{\Delta I_B}$	$\gamma = \frac{\Delta I_E}{\Delta I_B}$
Application	Multi stage amplifier	Audio signal amplifier	Impedance matching

Transistor as an Amplifier:

Transistor acts as an amplifier in active region. Let us see that how the transistor configuration acts as an amplifier.



Let us consider the voltage gain

$$A_V = \frac{V_o}{V_i}$$

$$but\ V_o = I_C R_C \text{ ---------- (1)}$$

$$\alpha = \frac{I_C}{I_E}$$

$$I_C = \alpha\, I_E \text{ ---------- (2)}$$

Substituting eq.2 in 1, we get,

$$V_o = \alpha\, I_E R_C$$

From the circuit, input voltage is $V_i = I_E r_e$

$$\text{Where } r_e \textit{ is the internal emitter resistance}$$

$$A_V = \frac{V_o}{V_i} = \frac{\alpha\, I_E R_C}{I_E r_e} = \frac{\alpha R_C}{r_e}$$

$$\text{Let us consider, } \alpha = 0.98, r_e = 40\Omega \textit{ and } R_C = 4K\Omega$$

$$A_V = \frac{\alpha R_C}{r_e} = \frac{0.98 * 4000}{40} = 98$$

Input signal applied to the amplifier is $V_i = 10mV$

$$A_V = \frac{V_o}{V_i}$$

$$V_o = A_V V_i = 98 * 10mV = 0.98\, Volts$$

Transistor Junction voltages:

Material	V_{BE}(Cutoff)	V_{BE}(Cutin)	V_{BE}(Act)	V_{BE}(Sat)	V_{CE}(Sat)
Si	0 V	0.5 V	0.6 V	0.7 V	0.3 V
Ge	-0.1 V	0.1 V	0.2 V	0.3 V	0.1 V

Field Effect Transistor (FET):

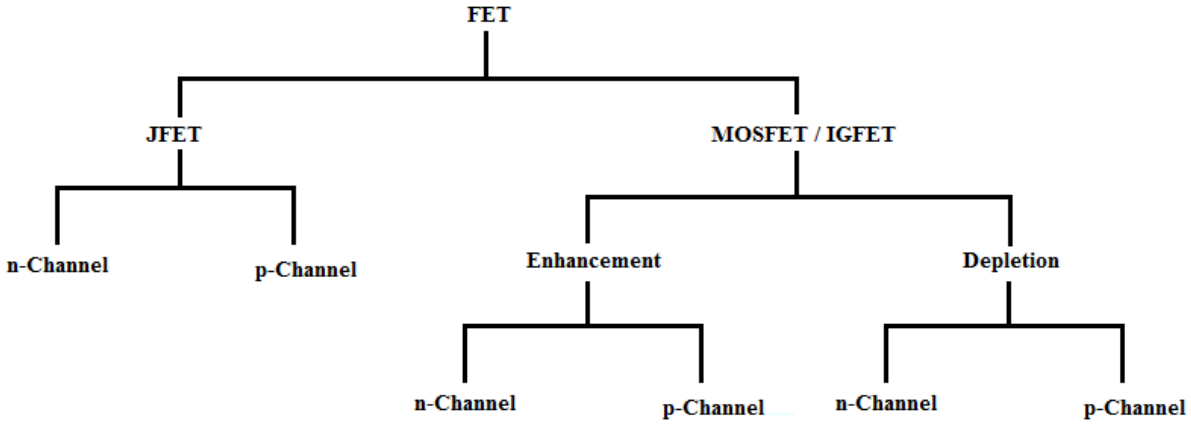
Advantages of FET over BJT:

1. In FET, current conduction is because of majority charge carriers. Hence, FET is called as uni-polar device.
2. FET is a voltage controlled device, where as BJT is a current controlled device.
3. FET has high input resistance compared with BJT.
4. FET provides better thermal stability.
5. It produces low noise during its operation.

Classification of FET:

FET's are classified into two types, they are

1. JFET (Junction Field Effect Transistor)
2. MOSFET (Metal Oxide Semiconductor Field Effect Transistor) or IGFET (Insulated Gate Filed Effect Transistor).



JFETs consist of three terminals namely, Source (S), Gate (G) and Drain (D). These devices are also called voltage controlled devices as the voltage applied at the gate terminal determines the amount of current flowing in-between the drain and the source terminals.

n-Channel JFET:

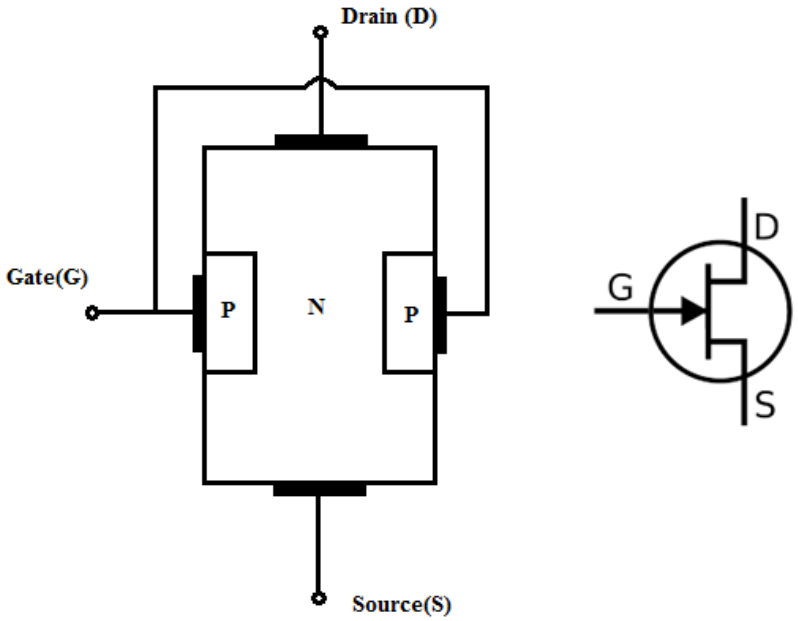


Figure: Semiconductor and symbolic representation of n channel JFET

The basic structure and symbol for n channel JFET is shown in the above figure. In n channel JFET, current conduction is because of electrons. Charge carriers flows from source

to drain. The flow of charge carriers from source to drain is controlled by gate terminal. Gate is normally reverse biased. The polarity of source and drain terminals depends on the channel type. Here, charge carriers moving from source to drain are controlled by varying the gate voltage, and hence it is called as voltage current controlled device.

Biasing and working of n channel JFET:

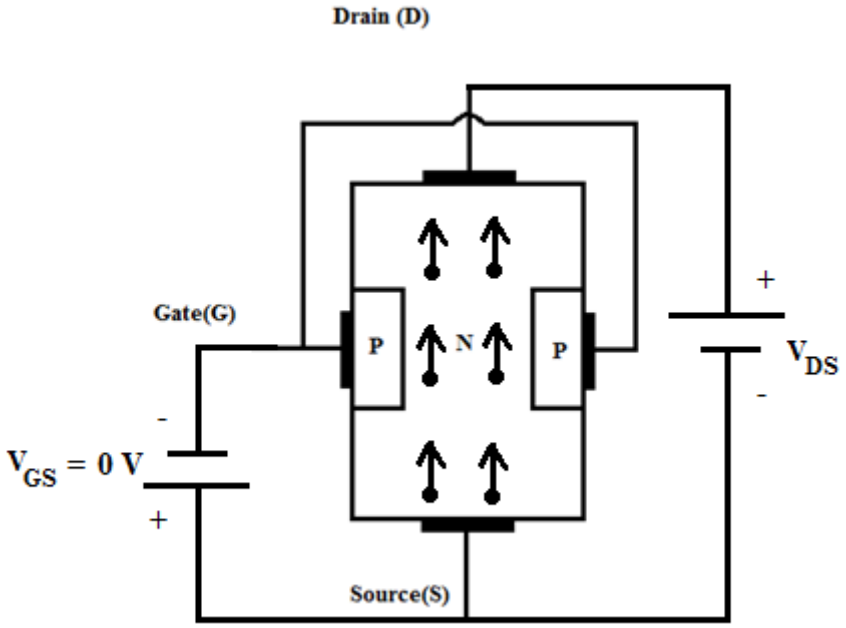


Figure: V_{GS} is made equal to '0'

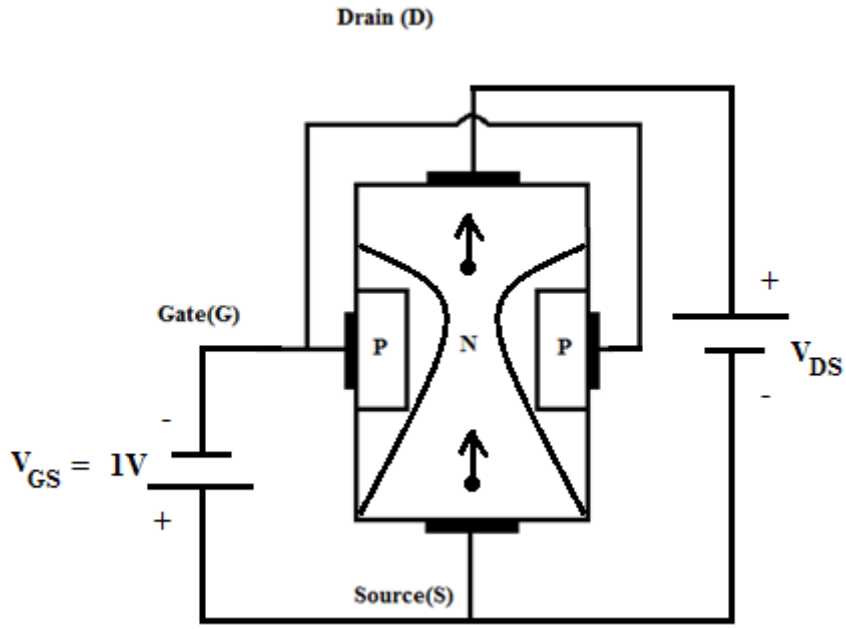


Figure: V_{GS} is slightly increased

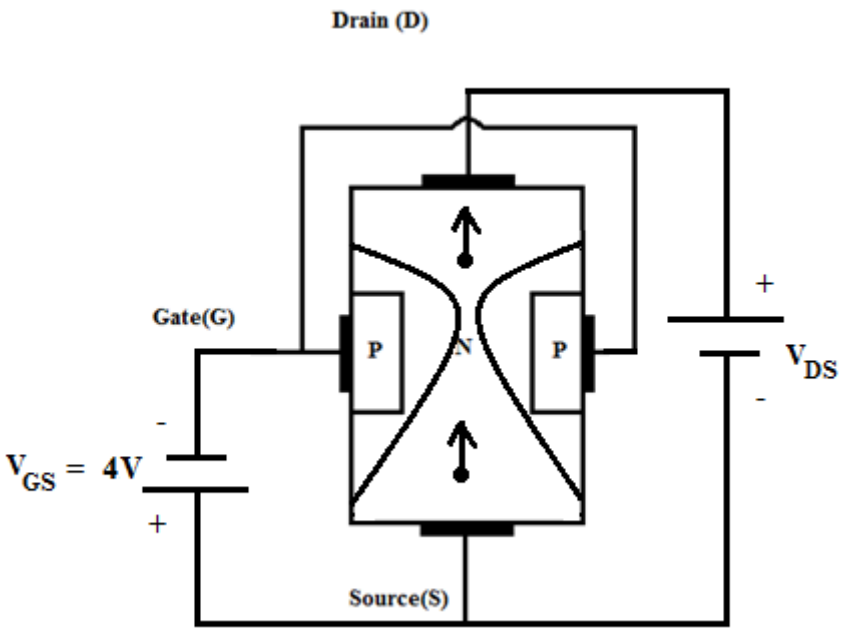


Figure: V_{GS} is increased more

The internal diagram for N-channel JFET transistor is shown above. This is a transistor with N-type of channel and with P-type materials of the region. If the gate is diffused into the N-type channel, then a reverse biased PN-junction is formed which results a depletion region around the gate terminal when no external supply is applied to the transistor. Generally the JFETs are called as depletion mode devices.

Gate is normally reverse biased. The biasing between source to drain is arranged in such a way that charge carriers moves from source to drain. Because of the biasing arrangement depletion width is more between drain and source, because drain to gate is more reverse biased compared to source to gate. Initially V_{GS} is made equal to zero; hence maximum channel width is available between source and drain. When V_{DS} is increased, number of charge carriers flows from source to drain increases and hence maximum drain current (I_D) will flow. If we will increase more negative voltage at the gate terminal then it reduces the channel width until no current flows through the channel. Now at this condition the JFET is said to be "pinched-off". The applied voltage at which the channel of FET closes is called as "pinched-off voltage (V_P)".

If the drain to source voltage (V_{DS}) is high enough, then the channel of the JFET breaks down and in this region uncontrolled maximum current passes through the device.

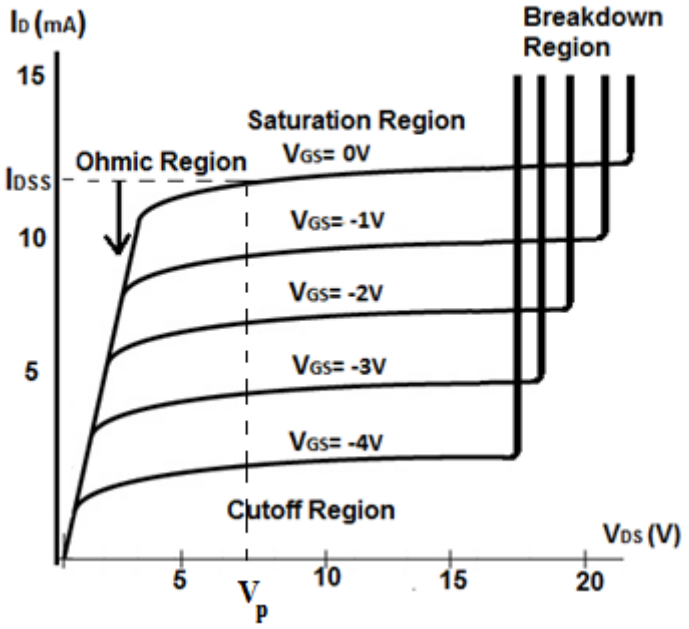


Figure: V-I Characteristics of FET

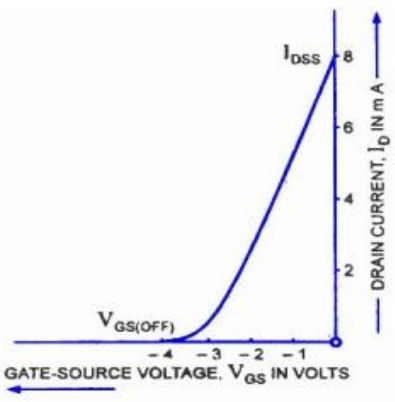
The JFET has different characteristics at different stages of operation depending on the input voltages and the characteristics of JFET at different regions are explained below. Mainly the JFET operates in ohmic, saturation, cut-off and break-down regions.

Ohmic Region: If V_{GS} = 0 then the depletion region of the channel is very small and in this region the JFET acts as a voltage controlled resistor.

Pinched-off Region: This is also called as cut-off region. The JFET enters into this region when the gate voltage is large negative, then the channel closes i.e.no current flows through the channel.

Saturation or Active Region: In this region the channel acts as a good conductor which is controlled by the gate voltage (V_{GS}).

Breakdown Region: If the drain to source voltage (V_{DS}) is high enough, then the channel of the JFET breaks down and in this region uncontrolled maximum current passes through the device.
The transfer characteristics of n channel JFET is shown is shown below.



Transfer characteristics shows that, at zero gate voltage, maximum drain current will flow and is represented with I_{DSS} and if the gate voltage is increased, drain current decreases and becomes zero at a particular voltage and this voltage is represented with $V_{GS\,(OFF)}$.

The drain current I_D flowing through the channel is zero when applied voltage V_{GS} is equal to pinch-off voltage V_P. In normal operation of JFET the applied gate voltage V_{GS} is in between 0 and V_P, In this case the drain current I_D flowing through the channel can be calculated as follows.

$$I_D = I_{DSS}\,(1-(V_{GS}/V_P))^2$$

Where, I_D = Drain current
I_{DSS} = maximum saturation current
V_{GS} = gate to source voltage
V_P = pinched-off voltage

The working of P channel JFET is similar to n channel except that the gate voltage is positive.

JFET parameters:

1. Drain resistance (r_d):

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D} \,/\, V_{GS}\ constant \qquad ohms$$

2. Trans conductance (or) Mutual Conductance (g_m):

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \,/\, V_{DS}\ constant \qquad mhos$$

3. Amplification factor (μ):

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \,/\, I_D\ constant$$

$$\mu = g_m r_d$$

Applications of JFET:

1. It is used as voltage variable resistor.
2. It is used in RF amplifiers.
3. JFET is used as an oscillator.
4. JFETs are popularly used in digital circuits like computers and memory elements because of small size.

Metal Oxide Semiconductor FET or Insulated Gate FET (MOSFET or IGFET):

The **IGFET** or **MOSFET** is a voltage controlled field effect transistor that differs from a JFET in that it has a "Metal Oxide" Gate electrode which is electrically insulated from the main semiconductor n-channel or p-channel by a very thin layer of insulating material usually silicon dioxide, commonly known as glass.

MOSFET's are classified into two types, they are

(1) Enhancement MOSFET
(2) Depletion MOSFET

In enhancement MOSFET channel does not exist from source to drain and is created. Whereas in depletion MOSFET, available channel is depleted. Again these MOSFET's are classified based on n channel or p channel.

(a) n channel enhancement MOSFET
(b) p channel enhancement MOSFET
(c) n channel depletion MOSFET
(d) p channel depletion MOSFET

n channel enhancement MOSFET:

In this MOSFET, channel doesn't exist between source and drain. This results in the device being normally "OFF" (non-conducting) when the gate bias voltage, V_{GS} is equal to zero. The circuit diagram and its symbol are shown below. Broken channel line to signify a normally open non-conducting channel between source and drain.

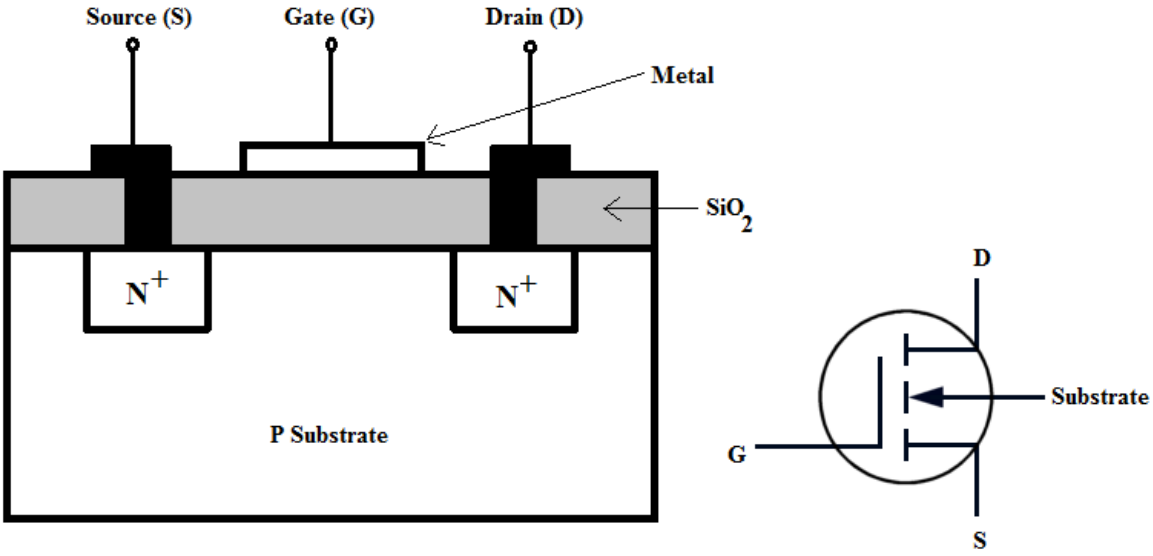


Figure: Basic diagram for n channel enhancement MOSFET and its symbol

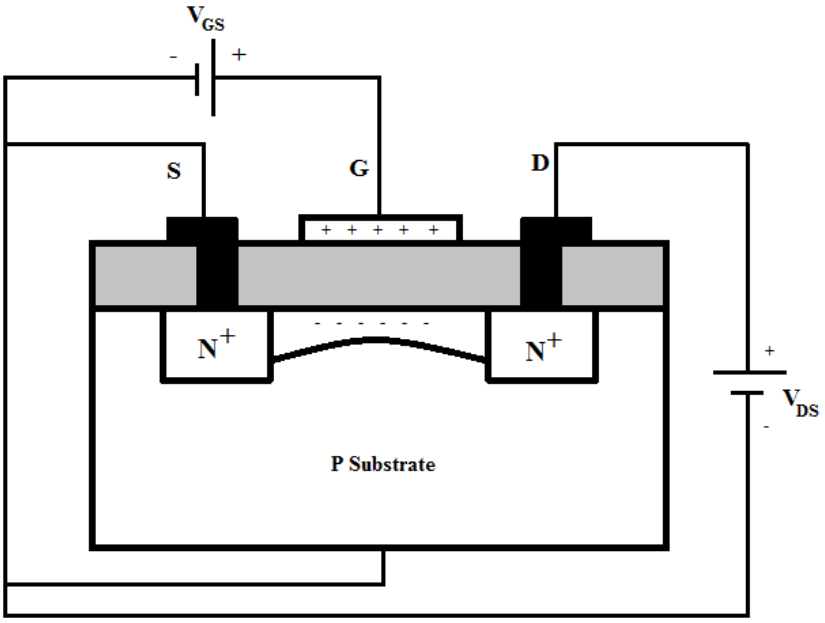


Figure: Working of n channel MOSFET

For the n-channel enhancement MOS transistor a drain current will only flow when a gate voltage (V_{GS}) is applied. The application of a positive (+ve) gate voltage to a n-type MOSFET attracts more electrons towards the oxide layer around the gate thereby increasing or enhancing (hence its name) the thickness of the channel allowing more charge carriers to flow from source to drain and hence drain current to flow. Because of this operation, the transistor is called an enhancement mode device as the application of a gate voltage enhances the channel.

Increasing this positive gate voltage will cause the channel resistance to decrease further causing an increase in the drain current, I_D through the channel. In other words, for an n-channel enhancement mode MOSFET: $+V_{GS}$ turns the transistor "ON", while a zero or negative V_{GS} turns the transistor "OFF". Then, the enhancement-mode MOSFET is equivalent to a "normally-open" switch.

V-I characteristics of n channel enhancement MOSFET is shown in the following figure.

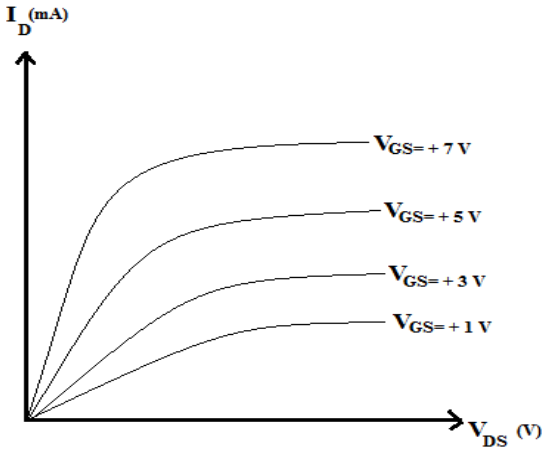


Figure: V-I characteristics of n channel enhancement MOSFET

n channel Depletion MOSFET:

In this MOSFET, n channel exists between source and drain. This results in the device being normally "ON" (conducting), V_{GS} is equal to zero. The circuit diagram and its symbol are shown below. Solid channel line to signify a normally closed conducting channel between source and drain.

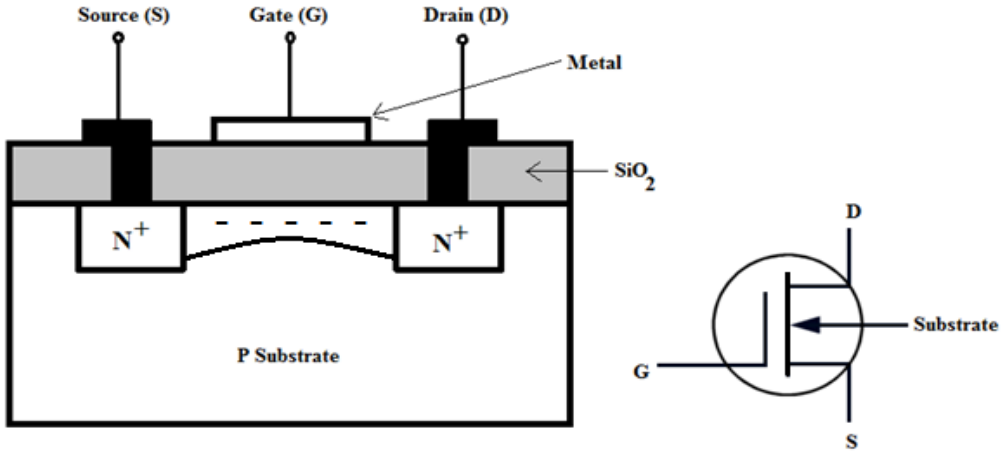


Figure: Basic diagram for n channel depletion MOSFET and its symbol

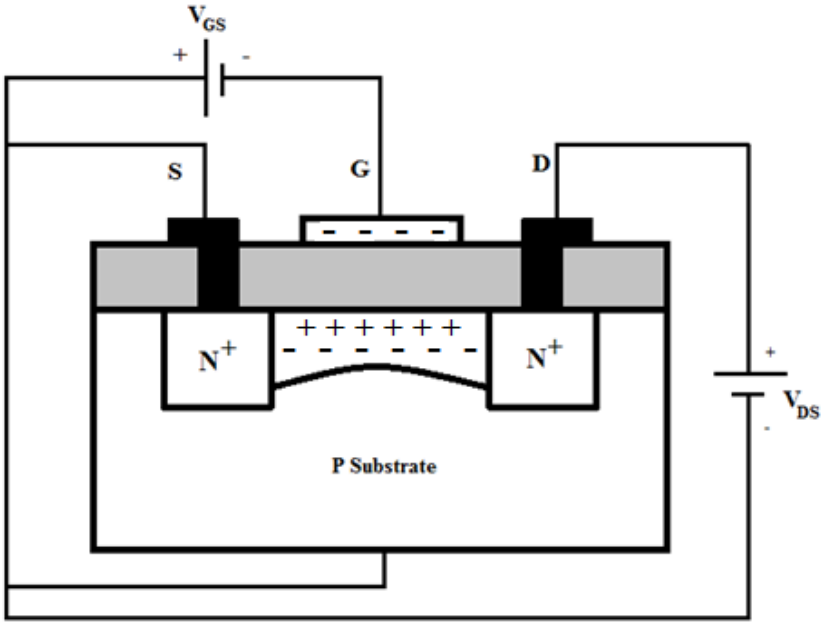


Figure: Working of n channel depletion MOSFET

For the n-channel depletion MOS transistor a drain current is maximum when gate voltage (V_{GS}) is zero. Under this condition the available channel width is maximum between source and drain. The application of a positive (-ve) gate voltage to a n-type MOSFET creates a positive charge in the n channel as a result, its width decreases. If the gate voltage is further increased, correspondingly channel width decreases, which reduce the carrier flow from source to drain causing drain current to decrease. Because of this operation, the transistor is called a depletion mode device as the application of a gate voltage depletes the channel.

Increasing this negative gate voltage will cause the channel resistance to increase further causing an decrease in the drain current, I_D through the channel. In other words, for an n-channel depletion mode MOSFET: $-V_{GS}$ turns the transistor "OFF". Then, the depletion-mode MOSFET is equivalent to a "normally-closed" switch.

V-I characteristics of n channel depletion MOSFET is shown in the following figure.

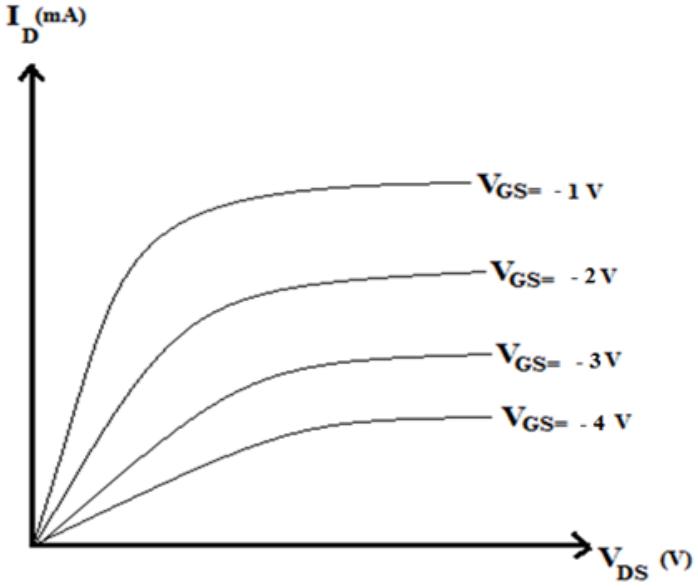


Figure: V-I characteristics of n channel depletion MOSFET

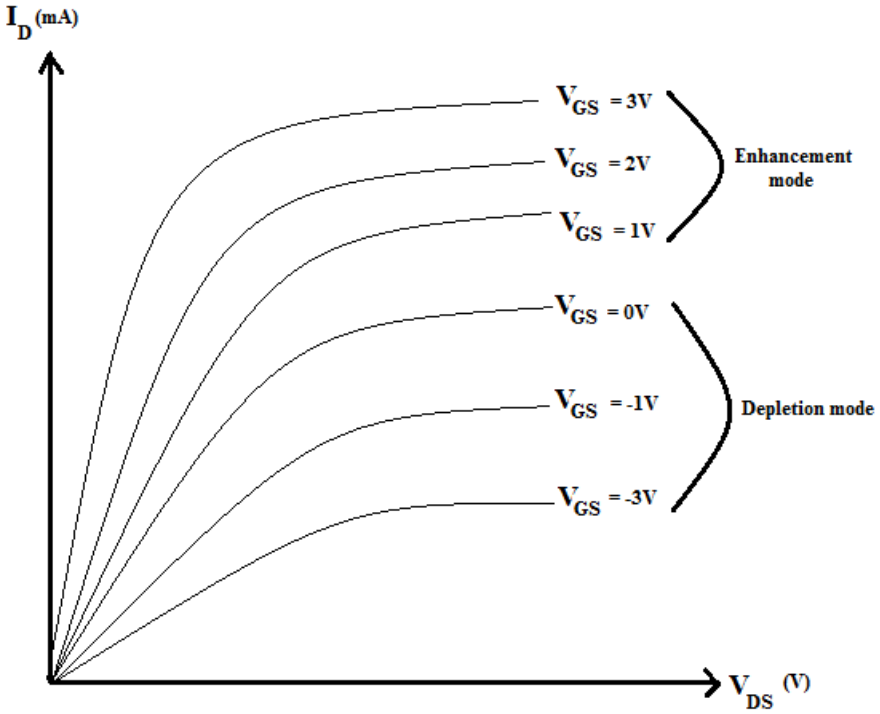


Figure: Combination of depletions and enhancement mode of MOSFET

The transfer characteristics of MOSFET is shown below

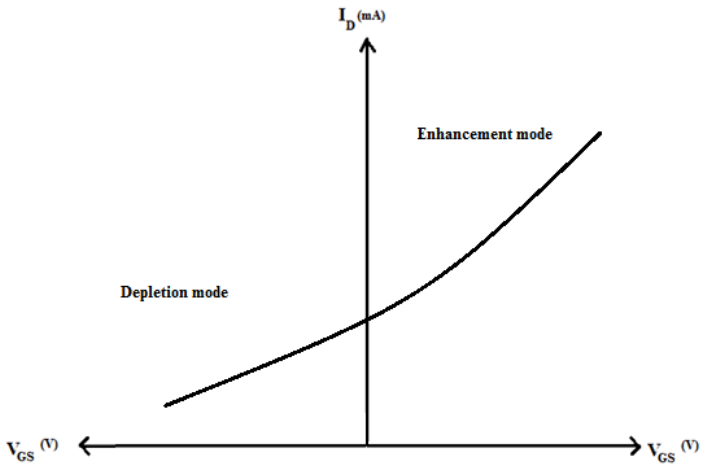


Figure: transfer characteristics of MOSFET

Comparison between JFET and MOSFET:

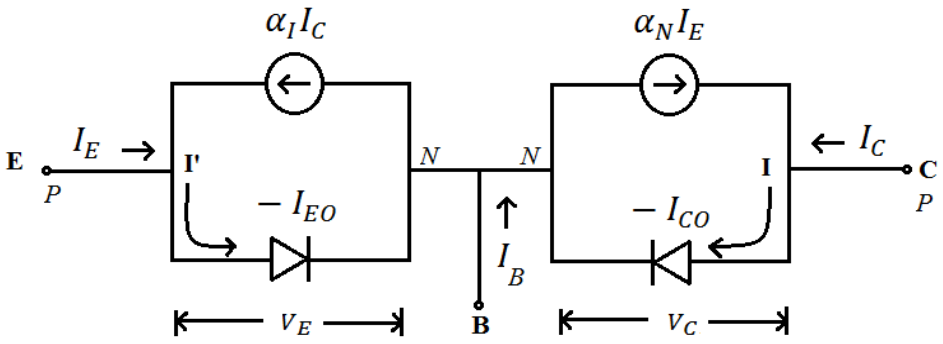
1. JFET is operated only in depletion mode, where as MOSFET can be operated in depletion as well as in enhancement mode.
2. Fabrication of MOSFETs is easier compared to JFETs.
3. JFET has high input impedance compared with MOSFET.
4. In JFET, electric field is created across reverse biased PN junction, where as in MOSFET electric field is created between gate and semiconductor.
5. If MOSFET is not handled properly, there is a possibility for damage when compared with JFET.

Ebers – Moll model of a transistor:

The general expression for collector current is given by

$$I_C = -\alpha_N I_E - I_{CO}\left(e^{V_C/V_T} - 1\right)$$

$$I_E = -\alpha_I I_C - I_{EO}\left(e^{V_E/V_T} - 1\right)$$



$$I_C = -\alpha_N I_E + I$$

$$I_C = -\alpha_N I_E + I_o\left(e^{V/V_T} - 1\right)$$

$$I_C = -\alpha_N I_E - I_o\left(e^{V_C/V_T} - 1\right)$$

Photo Transistor:

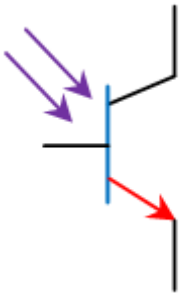


Figure: Symbol for photo transistor

The base of the photo transistor would only be used to bias the transistor so that additional collector current was flowing and this would mask any current flowing as a result of the photo-action. For operation the bias conditions are quite simple. The collector of an n-p-n transistor is made positive with respect to the emitter or negative for a p-n-p transistor.

The light enters the base region of the phototransistor where it causes hole electron pairs to be generated. This mainly occurs in the reverse biased base-collector junction. The hole-electron pairs move under the influence of the electric field and provide the base current, causing electrons to be injected into the emitter. The V-I characteristics of phototransistor is shown below.

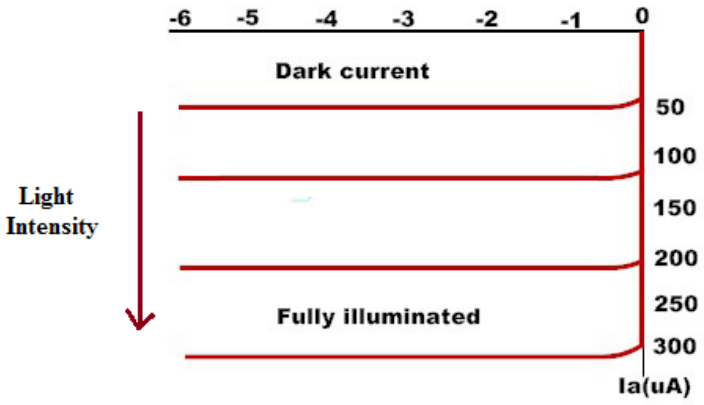


Figure: V-I Characteristics of Photo transistor